PCT CLAIMS:

1. A method of making an insulated electrical connection between a first (14) (top) and a second (16) (bottom) surface of a conducting or semi-conducting wafer, comprising

creating a trench in the first surface;

establishing an insulating enclosure entirely separating a portion of said wafer, defined by said trench, from surrounding material of said wafer, while exposing the top and bottom surfaces of said separated portion.

2. The method as claimed in claim 1, wherein said trench is defined by a pattern in the form of a closed loop, encircling a portion of said wafer but not extending through the wafer; and wherein said insulating enclosure is established by thinning said bottom surface so as to expose the insulating material in the trench, thereby establishing the insulating enclosure.

3. The method as claimed in claim 2, wherein the thinning is performed selectively on said surface so as to yield at least one depression in said surface, whereby at least one depression exhibits said electrical connections.

4. The method as claimed in claim 1, wherein said trench is defined by a pattern in the form of a line having a beginning and an end and extending through the substrate; and wherein said insulating enclosure is established by creating a second trench complementary to said first trench and extending through the wafer to define a pattern in the form of a closed loop; and by subsequently filling said second trench with insulating material.

5. The method as claimed in claim 1, wherein said trench is defined by a pattern in the form of a closed loop, encircling a portion of said wafer but not extending through the wafer; and wherein said insulating enclosure is established by creating a second trench from the bottom side and mating with said first trench; and by subsequently filling said second trench with insulating material.

6. The method as claimed in any preceding claim, wherein the trenches are created by an etching process.

7. The method as claimed in any preceding claim, wherein the trenches are created by a laser based machining process.

8. The method as claimed in any preceding claim, wherein the trenches are created by an electro-discharge machining process.

9. The method as claimed in any preceding claim, wherein insulating material is introduced in said trenches.

10. The method as claimed in claim 9, wherein said trenches at least partially are filled with said insulating material.

11. A method of making an insulated electrical connection between a first and a second surface of a wafer, comprising

providing a wafer of a suitable conducting or semi-conducting material;

etching at least one trench in said wafer from at least one surface, said trench completely surrounding a portion of said wafer;

filling said trench with an insulating material thereby creating an insulated electrical connection extending through said wafer.

12. A method of making an insulated electrical connection between a first and a second surface of a wafer, comprising

providing a wafer of a suitable conducting or semi-conducting material;

etching at least one trench from the first surface, said trench completely surrounding a portion of said wafer;

filling said trench with an insulating material; and

thinning said wafer from the second surface to expose the insulating material in said trench, thereby creating an insulated electrical connection extending through said wafer.

13. A method of making an insulated electrical connection between a first and a second surface of a wafer, comprising

providing a wafer of a suitable conducting or semi-conducting material;

etching at least one trench from the first surface, said trench completely surrounding a portion of said wafer;

filling said trench with an insulating material;

etching at least one further trench from the second surface, said trench completely surrounding a portion of said wafer matching/corresponding to/in alignment with said portion on the first surface;

filling said further trench with an insulating material.

14. A method o making an electrical connection between a first and a second surface of a wafer as claimed in any preceding claim, comprising introducing a doping material into a trench, for selectively doping the material surrounded by the trench.

15. The method as claimed in claim 14, wherein at least one further trench or hole is provided in the wafer in the region surrounded by said trench to enable the provision of a deeper doping.

16. The method as claimed in claim 3, wherein the wafer comprises an etch stop layer provided at a depth corresponding to the bottom of said cavity, whereby the trenches are etched to a predetermined depth, defined by said etch stop layer, and wherein the thinning of the wafer comprises removing said etch stop layer.

17. A product (10) usable as a starting substrate for the manufacture of micro-electronic and/or micro-mechanic devices, comprising

a wafer (10) of a semi-conducting or conducting material, and having a first (14) and a second (16) surface;

at least one electrically conducting member (12) extending through said wafer,

characterized in that

the electrically conducting member (12) is insulated from surrounding material of the wafer by a finite layer (15) of an insulating material; and in that

it comprises the same material as the wafer, i.e. it is made from the wafer material.

18. The product as claimed in claim 17, wherein said wafer is a semiconductor wafer.

19. The product as claimed in claim 18, wherein said wafer is a silicon wafer.

20. The product as claimed in any of claims 16-19, wherein said wafer has a thickness of 200 – 5000 μm, preferably 300 - 3000 μm, most preferably 400 - 1000 μm.

21. The product as claimed in any of claims 16-20, wherein the thickness of the finite layers of insulating material is 1-20 μm, typically 8-12 μm.

22. The product as claimed in any of claims 16-21, wherein the pitch/center-to-center distance between the electrical connections is larger than 10 μm, typically 50-100 μm.

23. The product as claimed in any of claims 16-22, wherein the wafer is essentially flat.

24. The product as claimed in any of claims 16-22, wherein the wafer comprises one or more local depressions (75) in at least one surface thereof, wherein the insulated electrical connections are essentially flush with the bottom surface of said depressions.